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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,356	02/11/2004	Wei-Chieh Hsuch	3304.2.119	3184

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EXAMINER	
SHAPIRO, LEONID	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/776,356	HSUEH, WEI-CHIEH	
	Examiner	Art Unit	
	Leonid Shapiro	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8-11 and 16-20* is/are rejected.

7)☒ Claim(s) *4-7 and 12-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 4-24-06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3,8-11,16-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Yumoto (6,859,193).

As to claim 1, Yumoto teaches a pixel driving circuit for use in an active matrix electron luminescent display, switched between a memorizing state and an emission state according to operations of a first and a second scan lines (fig. 13, scanA,scanB, TFT1,TFT3-TFT5,OLED, from col. 18,line 60 to col. 19, line 15), comprising:

a transistor (fig. 13, item TFT1);

a capacitor having a first and a second ends coupled to the gate electrode of said transistor and a ground voltage (fig. 13, items C,TFT1), respectively; and

an organic light-emitting diode having a P and an N electrode coupled to the source electrode of said transistor and said ground voltage, respectively (fig. 13, items OLED,TFT1),

wherein said capacitor is charged by a driving current received from a data line to generate a specified voltage to bias said transistor and said organic light-emitting diode in said memorizing state, and said transistor and said organic light-emitting diode are

further biased with said specified voltage in said emission state (from col. 18,line 60 to col. 19, line 15).

As to claim 9, Yumoto teaches a pixel driving circuit for use in an active matrix electron luminescent display, switched between a memorizing state and an emission state according to operations of a first and a second scan lines, comprising: a transistor; a capacitor having a first and a second ends coupled to the gate electrode of said transistor and a voltage source (figs 5-6, , scanA, scanB, TFT1 –TFT4,OLED, from col. 11,line 15 to col. 12, line 67), respectively; and

an organic light-emitting diode having a P and an N electrode coupled to said voltage source and the source electrode of said transistor (fig.5, items OLED,Vdd,TFT2), respectively,

wherein said capacitor is charged by a driving current transmitted from said voltage source to generate a specified voltage to bias said transistor and said organic light-emitting diode in said memorizing state, and said transistor and said organic light-emitting diode are further biased with said specified voltage in said emission state (col. 12, lines 28-67).

As to claim 17, Yumoto teaches a method for driving a pixel unit of an active matrix electron luminescent display, said pixel unit comprising a capacitor, a transistor and an organic light-emitting diode (fig. 5, items C,OLED,TFT1-TFT4), said method comprising steps of:

forming a current path for a driving current to charge said capacitor to a specified voltage when said first scan line is operating (figs. 5-6, items CS,TFT,C, col. 12, lines

28-44) ; and

generating a biasing current in response to said specified voltage to pass through said organic light-emitting diode when said second line is operating (figs. 5-6, items TFT,C, col. 12, lines 45-67),

wherein said specific voltage biases the gate electrode of said transistor and said organic light-emitting diode serially coupled to each other (col. 12, lines 45-67).

As to claims 2,10,18 Yumoto teaches a memorizing state circuit coupled to said first scan line, said data line, the gate electrode of said transistor and the drain electrode of said transistor, and permitting said driving current from said data line to be transmitted there via to charge said capacitor and pass through said transistor and said organic light-emitting diode in said memorizing state (figs. 5-6, items CS,TFT,C, col. 12, lines 28-44).

As to claims 3,11,19 Yumoto teaches an emission state circuit coupled to a voltage source, the drain electrode of said transistor and said second scan line, and generating a current in response to said specified voltage to pass through said transistor and said organic light-emitting diode in said emission state (figs. 5-6, items TFT,C, col. 12, lines 45-67).

As to claims 8, 16 Yumoto teaches pixel driving circuit is switched between said memorizing state and said emission state in response to a clock signal for controlling said operations of said first and said second scan lines (fig. 7, items VCKA,VCKB, col. 13, lines 48-65).

As to claim 20 Yumoto teaches the N electrode of said organic light-emitting diode is coupled to the drain electrode of said transistor, said capacitor has a first and a second end coupled to the gate electrode of said transistor and the P electrode of said organic light-emitting diode, and each of said driving current and said biasing current passes through the source and the drain electrode of said transistor (figs. 5-6, items TFT,C, col. 12, lines 45-67).

Allowable Subject Matter

3. Claims 4-7, 12-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claim 4,6,12,14 the major difference between the teaching of the prior art of record (Yumoto) and the instant invention is that a second switch unit having a third and a fourth ends coupled to the drain electrode and the gate electrode of said transistor, respectively, and a second control end coupled to said first scan line.

Claims 5,7,13,15 depend on claims 4,6,12,14.

Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LS
05.15.07

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